Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, NOV/DEC 2025

Third Semester

Computer Science and Engineering

UECTL24302 - Digital Principles and Computer Organization

(Common to Information Technology & Artificial Intelligence and Data Science)

Regulations - 2024

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	Define minterm and maxterm.	L1	1	2
2.	Differentiate decoder and encoder.	L2	1	2
3.	What is a flip-flop?	L1	2	2
4.	Differentiate Moore and Mealy model.	L2	2	2
5.	What are basic operations of a computer memory?	L1	3	2
6.	Distinguish between auto increment and auto decrement addressing mode.	L2	3	2
7.	Define delayed branching.	L1	4	2
8.	How can we eliminate the delay in data hazard?	L2	4	2
9.	Differentiate Temporal Locality of Reference and Spatial Locality of Reference.	L2	5	2
10.	Define bus arbitration. List out its types.	L1	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a		Construct full adder with two half adders and an OR gate.	L3	1	16
			Or			
	b	i	Implement a 2-bit comparator using truth table and logic circuit.	L3	1	8
		ii	Draw a 4:1 Mux and implement the following function F= (0,1,2,4,6,9,12,14).	L3	1	8
12.	a		Implement a BCD counter that counts in the following way: 0000, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001 and back to 0000.	L3	2	16
			Or			
	b		A sequential circuit with two D flip-flops A and B, one input x, and one output z is specified by the following next state and output equations: A(t+1) = A'+B, B(t+1) =B'X, Z =A+B' i. Draw the logic diagram of the circuit ii. Derive the state table iii. Draw the state diagram of the circuit	L3	2	16

13.	a	i	Explain Von Neumann Architecture in detail with diagram.	L2	3	10
		ii	Explain how instructions are categorized based on operations.	L2	3	6
			Or			
	b		Explain different addressing modes required to calculate the effective address of the operand with diagrams.	L2	3	16
14.	a		Describe the data path while executing an instruction with necessary diagrams in detail.	L2	4	16
			Or			
	b	i	Compare hardwired control and microprogrammed control unit.	L2	4	8
		ii	Explain different ways to resolve data hazard in a pipeline.	L2	4	8
15.	a	i	Explain in detail virtual memory is used for address translation.	L2	5	10
		ii	Compare Serial interface and parallel interface.	L2	5	6
			Or			
	b	i	Explain Cache memory mapping techniques.	L2	5	10
		ii	Describe how an interrupt is processed with necessary diagrams.	L2	5	6